26.3 A 20mW 3.24mm² Fully Integrated GPS Radio for Cell-Phones

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A very steep growth in location-related services is foreseen in the next few years by industry analysts. Cellular phones with embedded GPS engines will enable network-based positioning methods. Assisted GPS solutions allow a direct migration path into 3G handsets besides being more accurate than cell tower-based ones. Co-existence of a GPS receiver together with cell-phones on the same PCB poses new challenges. In applications where GPS receiver is concurrent with the cellular phone, signals leaking from the transmitter are dangerous interferers. Moreover, minimum power consumption is the key, because the GPS radio is always on, and small form factor is fundamental to simplify the application board. In this paper, a fully integrated GPS radio, not requiring any external filter, yet being robust to the large transmitter leakage is presented. Prototypes are realized in 0.18µm SiGe BiCMOS technology. The die area is 3.24mm² and the power consumption is 20mW. The blocking power causing 1dB gain desensitization at 1.9GHz is -8dBm.

The block diagram is shown in Fig. 26.3.1. The RF front-end comprises an LNA, quadrature mixers, and a fully integrated synthesizer. In the IF strip, poly-phase filters are followed by a VGA with dc-offset control loop and an ADC. Minimizing the effect of leakage from the cell-phone transmitter into the GPS receiver side drives the frequency planning and the design choice of the RF front-end. Low-IF has emerged as the architecture of choice for this application, because it allows high level of integration and it is robust to dc offset and low-frequency noise. Furthermore, it easily interfaces with most digital baseband modules [1, 2]. To eliminate the problem of second order intermodulation distortion products, extending from dc to 2BW where BW is the signal bandwidth, a 4MHz IF is chosen. The solution is amenable for 3G systems like WCDMA. Furthermore, this choice of low IF results in an image signal that is still within the GPS band. Thermal noise only needs to be rejected in the image band.

The achievable sensitivity is limited by the triplexer loss, mandating an external LNA to minimize the impact of the IC noise figure. Given the typical triplexer filtering profile, elimination of the usually adopted RF filter is feasible, provided the receiver is able to tolerate cell-phones blocking signals in the order of -10dBm to -5dBm. In the proposed scheme, filtering and gain are interleaved in the RF stage. As shown in Fig. 26.3.2, a notch filter at blocking frequency is followed by a voltage-voltage feedback LC-loaded LNA. The latter is chosen due to its superior linearity performance at given power consumption, over the inductively degenerated topology [3]. The notch filter is acting as a short at signal frequency. The input impedance is thus the load impedance reflected by the feedback loop. The second gain stage is based on a common-source input transconductor. The combined action of the input notch filter and selective LNA allows around 15dB blocker selectivity at 1.9GHz, greatly improving gain desensitization and reciprocal mixing. A passive mixer, driven by a quadrature VCO, down-converts the signal. The passive mixer is driven hard to assure good linearity and noise performance [4]. A digital automatic level-control loop is employed to set and maintain the desired output amplitude. The phase-noise requirement at large offsets, prohibitively high without frequency selection in the front-end, is still challenging (around -150dBc/Hz with -10dBm blocking power). Power consumption is nonetheless kept low, due to the high Q of passive components in the adopted process. To generate I and Q signals, the VCOs are locked in quadrature by means of a phase control loop, as shown in Fig. 26.3.3. This architecture is preferred to possible alternatives, due to its robustness against components mismatches in the VCOs. The available high-Q inductors allow low power consumption without a penalty in quadrature accuracy, which is only limited by mismatches in the mixer. The output frequency is synthesized by means of a fractional-N ΔΣ-based PLL, locked to an external crystal reference.

The IF strip is composed of a 2nd-order LPF followed by an active polyphase filter. The first LPF provides low-noise amplification of the IF signal while rejecting out-of-band noise and jammers. The active polyphase filter is implemented by two cascaded biquadratic cells, connected in a quadrature fashion, in order to reject noise in the image band. Both filters are based on opamps. A two-stage Miller configuration is adopted with both stages exploiting the high g_m/I of npn devices to achieve large unity-gain bandwidth together with low power consumption.

The filter is followed by the combination of a programmable attenuator and a VGA. The receiver can be tailored to the external LNA with various gain levels, by means of a 2b programmable attenuator that is able to re-align the received signal to the optimum level. The VGA has 30dB range to cover gain spreads due to process and temperature variations. An AGC loop, implemented with a charge pump driven by the magnitude bit, adjusts the gain of the VGA. A 2b quantizer follows.

The fully integrated GPS receiver, realized in a 0.18µm SiGe process, is housed in a QFN24 package. Figure 26.3.4 shows the chip micrograph. The die area, including bond pads, is 3.24mm², with the core cell occupying 2.56mm². The radio draws 11mA from a 1.8V supply. The output spectrum with a -110dBm input signal is shown in Fig. 26.3.5. The noise figure is 5dB. To evaluate tolerance to blocking signals around the received band, the 1dB gain desensitization is measured at various frequency offsets from 1.57GHz. Because the AGC adjusts the gain to have the proper signal level at the ADC input, the AGC output control voltage variation, corresponding to 1dB gain decrease, is detected. The result is plotted in Fig. 26.3.6, curve A. A second implementation of the GPS receiver, employing a conventional inductively degenerated LNA in place of the two-stage LNA of Fig. 26.3.2, is measured for comparison. The two LNAs have roughly the same gain but the proposed solution is much more tolerant to blocking signals at large frequency offset, as evident from curve B. The oscillator phase noise, measured at 1MHz offset from carrier, is -110dBc/Hz, while integrated phase noise is -25dBc. Figure 26.3.7 summarizes the results.

Acknowledgment:
The authors wish to thank Massimo Brandolini for helping with measurements.

References:
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[4] E. Sacchi, et al., "A 15mW, 70kHz 1/f Corner Direct Conversion CMOS Receiver" *Proc. IEEE CICC*, pp. 459-462, Sept., 2003.

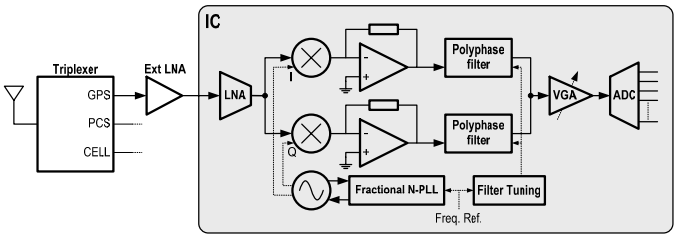

Figure 26.3.1: GPS radio block diagram.

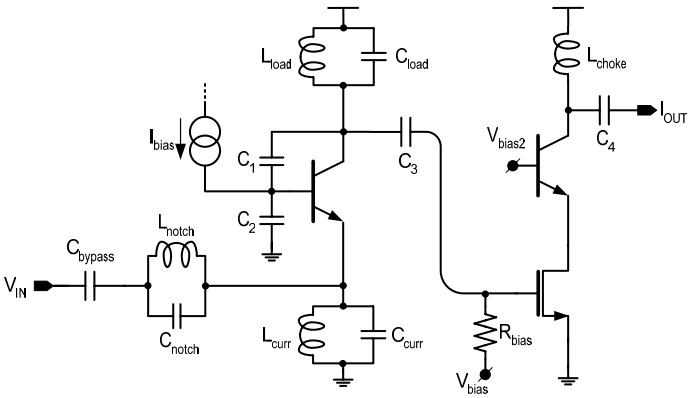

Figure 26.3.2: Two-stage LNA schematic.

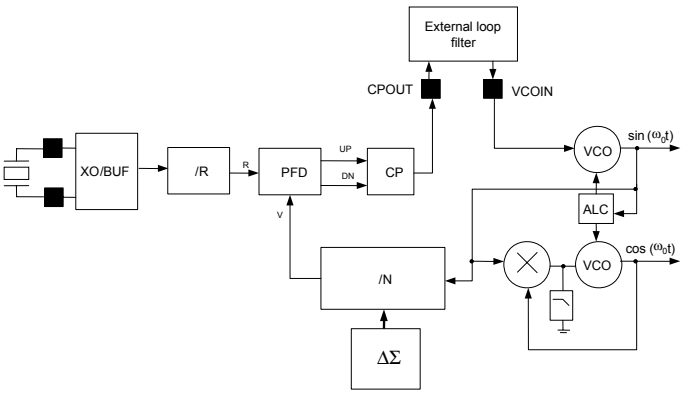

Figure 26.3.3: PLL block diagram.

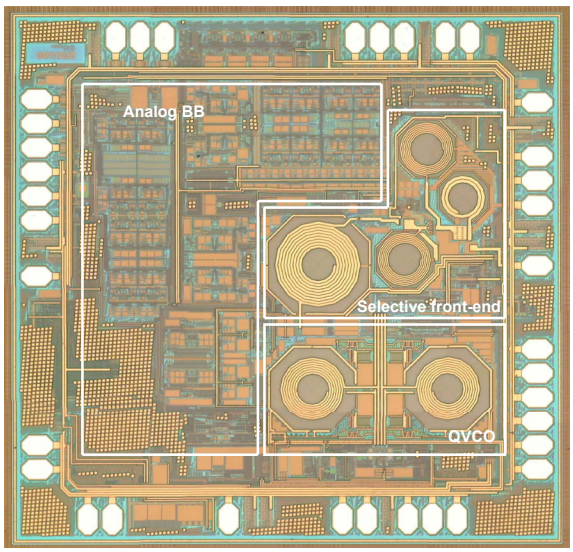

Figure 26.3.4: Die micrograph.

Figure 26.3.5: IF output spectrum with –110dBm input.

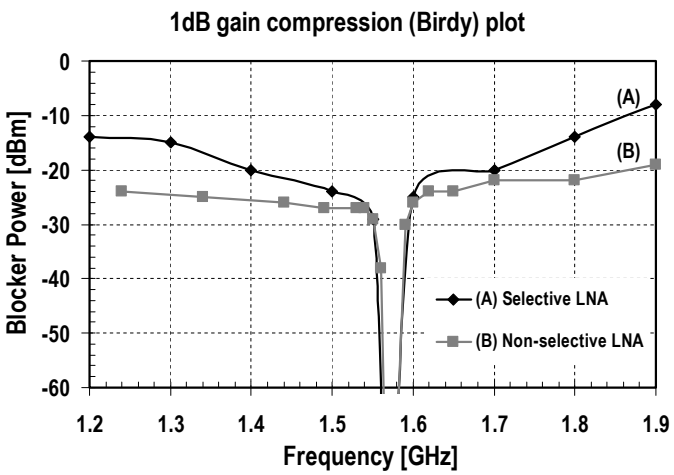

Figure 26.3.6: 1dB desensitization for this radio and a non-selective LNA-based radio.

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1dB desens @ 1.9GHz [dBm]	-8
Noise Figure [dB]	5
Phase Noise @ 1MHz [dBc/Hz]	-110
Voltage Supply [V]	1.8
Current consumption [mA]	11
Die area [mm^2]	3.2
Active area [mm^2]	2.5
Package	QFN24
Technology	SiGe 0.18μm CMOS

Figure 26.3.7: Measurement summary.

